



PST-360: Instructions for use

HOW TO ORDER: **PST360-1S-C0000-ERA360-05E**
 OUTPUT TYPE: **Simple - SPI Protocol**
 SIGNAL OUTPUT **10% to 90% SPI Protocol (360° ERA)**

ROTOR: **14mm**
 OUTPUT FUNCTION: **Curve 0000**

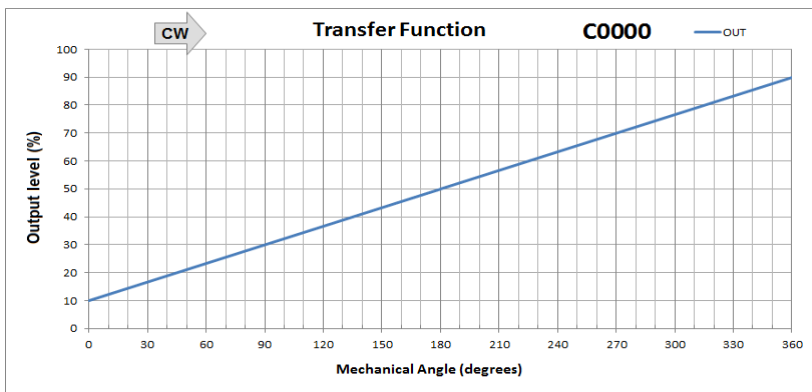
SUPPLY VOLTAGE: **5V ± 10%**
 TEMPERATURE: **-40 °C to +85 °C**

Connections scheme:

Wire color	Connection	Recommended connections
Brown	Power supply Vdd: 5V ± 10%	
Blue	Ground	
Black	MOSI	
White	/SS	
Grey	SCLK	

⚠ WARNING
 -In order to minimize the possibility of short circuits, we recommend to connect the power supply at the end

Signal output:



Reference position:

Rotor is shown at zero position



CLOCKWISE

To get more information about our full Legal Disclaimer and Limitation of Liability please visit www.piher.net/disclaimer_hollow_shaft.pdf.
 Users acknowledge that they have read this legal disclaimer and agree to abide by its terms.

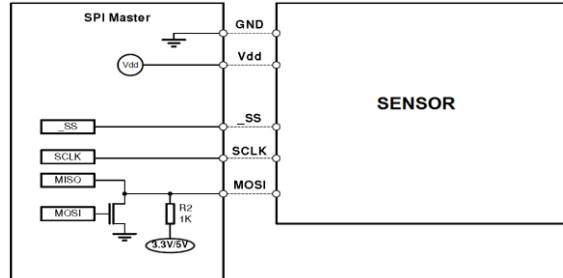
Piher Sensors & Controls SA *** confidential ***
 Poligono Industrial Municipal, Vial T2, No 22, 31500 Tudela, Navarra, Spain

Tel: +34 948 820 450
 Fax: +34 948 824 050
www.piher.net

Piher is an Amphenol[™] company.
 RM Navarra Tomo 551, Folio 7, Hoja 5.580
 CIF/VAT ESA31169907

The PST-360 features a digital Serial protocol mode. The PST-360 is considered as a Slave node. The serial protocol of the PST-360 is a three wires protocol (/SS, SCLK, MOSI-MISO):

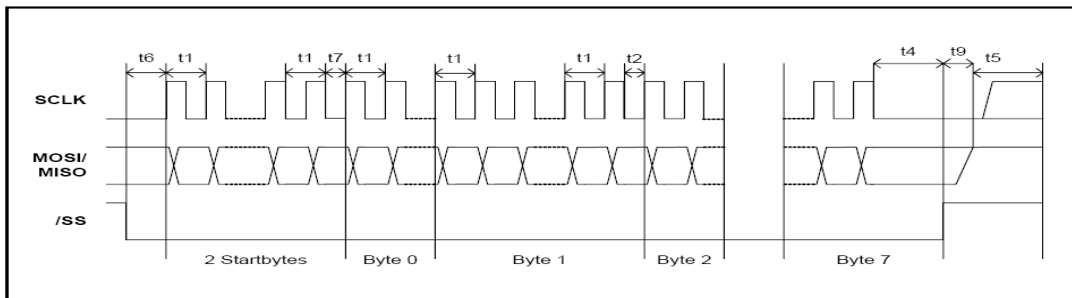
- /SS pin is a 5V tolerant digital input.
- SCLK pin is a 5V tolerant digital input.
- MOSI-MISO pin is a 5V tolerant open drain digital input/output.



1. Timing

To synchronize communication, the master deactivates /SS high for at least t_5 (1.5 ms). In this case, the Slave will be ready to receive a new frame. The master can re-synchronize at any time, even in the middle of a byte transfer.

Note: Any time shorter that t_5 leads to an undefined frame state, because the Slave may or may not have seen /SS inactive.



Timings	Min ⁽¹⁾	Max	Remarks
t1	6.9 μ s	-	No capacitive load on MISO. t1 is the minimum clock period for any bits within a byte.
t2	37.5 μ s	-	t2 the minimum time between any other byte.
t4	6.9 μ s	-	Time between last clock and /SS=high=chip de selection.
t5	1500 μ s	-	Minimum /SS=Hi time where it's guaranteed that a frame re-synchronizations will be started.
t5	0 μ s	-	Maximum /SS=Hi time where it's guaranteed that NO frame re-synchronizations will be started.
t6	6.9 μ s	-	The time t6 defines the minimum time between /SS=Lo and the first clock edge.
t7	45 μ s	-	t7 is the minimum time between the StartByte and the Byte0.
t9	-	< 1 μ s	Maximum time between /SS=Hi and MISO Bus High-Impedance.
T _{StartUp}	-	< 16 μ s	Minimum time between reset-inactive and any master signal change.

⁽¹⁾ Timings shown for oscillator base frequency of 7MHz (Slow mode)

2. Slave Reset

On internal soft failures the Slave resets after 1 second or after an (error) frame is sent. On internal hard failures the Slave resets itself. In that case, the Serial protocol will not come up. The serial protocol link is enabled only after the completion of the first synchronization (the Master deactivates /SS for at least 15).

3. Slave Start-Up

The Slave start-up (after power-up or an internal failure) takes 16 ms. Within this time /SS and SCLK is ignored by the Slave. The first frame can therefore be sent after 16 ms. MISO is Hi-Z (i.e. Hi-Impedance) until the Slave is selected by its /SS input. MTS-360 will cope with any signal from the Master while starting up.

To get more information about our full Legal Disclaimer and Limitation of Liability please visit www.piher.net/disclaimer_hollow_shaft.pdf.

Users acknowledge that they have read this legal disclaimer and agree to abide by its terms.

Piher Sensors & Controls SA *** confidential ***
Poligono Industrial Municipal, Vial T2, No 22, 31500 Tudela, Navarra, Spain

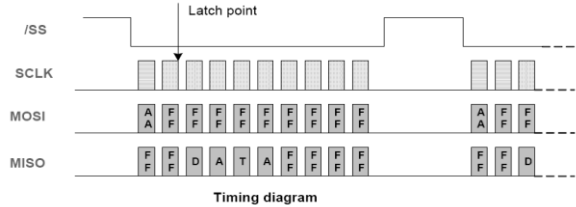
Tel: +34 948 820 450
Fax: +34 948 824 050
www.piher.net

Piher is an Amphenol[™] company.
RM Navarra Tomo 551, Folio 7, Hoja 5.580
CIF/VAT ESA31169907

4. Frame Layer

4.1. Command Device Mechanism

Before each transmission of a data frame, the Master should send a byte AAh to enable a frame transfer. The latch point for the angle measurement is at the last clock before the first data frame byte.



4.2. Data Frame Structure

A data frame consists of 10 bytes:

- 2 start bytes (AAh followed by FFh)
- 2 data bytes (DATA16 – most significant byte first)
- 2 inverted data bytes (/DATA16 – most significant byte first)
- 4 all-Hi bytes

The Master should send AAh (55h in case of inverting transistor) followed by 9 bytes FFh. The Slave will answer with two bytes FFh followed by 4 data bytes and 4 bytes FFh.

4.3. Timing

There are no timing limits for frames: a frame transmission could be initiated at any time. There is no inter-frame time defined.

4.4. Data structure

The DATA16 could be a valid angle, or an error condition. The two meanings are distinguished by the LSB.

DATA16: Angle A[13:0] with (Angle Span)/2¹⁴

Most Significant Byte								Less Significant Byte							
MSB							LSB	MSB							LSB
A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	0	1

DATA16: Error

Most Significant Byte								Less Significant Byte							
MSB							LSB	MSB							LSB
E15	E14	E13	E12	E11	E10	E9	E8	E7	E6	E5	E4	E3	E2	E1	E0

BIT	NAME	
E0	0	
E1	1	
E2	F_ADCMONITOR	ADC Failure
E3	F_ADCSATURA	ADC Saturation (Electrical failure or field too strong)
E4	F_RGTOOLOW	Analog Gain Below Trimmed Threshold (Likely reason : field too weak)
E5	F_MAGTOOLOW	Magnetic Field Too Weak
E6	F_MAGTOOHIGH	Magnetic Field Too Strong
E7	F_RGTOOHIGH	Analog Gain Above Trimmed Threshold (Likely reason : field too strong)
E8	F_FGCLAMP	Never occurring in serial protocol
E9	F_ROCLAMP	Analog Chain Rough Offset Compensation : Clipping
E10	F_MT7V	Device Supply VDD Greater than 7V
E11	-	
E12	-	
E13	-	
E14	F_DACMONITOR	Never occurring in serial protocol
E15	-	

4.5. Angle Calculation

All communication timing is independent (asynchronous) of the angle data processing. The angle is calculated continuously by the Slave:

- Slow mode: every 1.5 ms at most.

The last angle calculated is hold to be read by the Master at any time. Only valid angles are transferred by the Slave, because any internal failure of the Slave will lead to a soft reset.

4.6. Error handling

In case of any errors listed in the previous table, the Serial protocol will be initialized and the error condition can be read by the master. The Slave will perform a soft reset once the error frame is sent.

In case of any other errors (ROM CRC error, EEPROM CRC error, RAM check error, intelligent watchdog error ...) the Slave's serial protocol is not initialized. The MOSI/MISO pin will stay Hi-impedant (no error frames are sent).